IN THE SPECIFICATION

1. On page 1, lines 2-3 of the specification, please amend the title of the application as follows:

B1

-- METHOD AND APPARATUS FOR MULTI-MODE JUMP DELAY SLOT CONTROL IN A PIPELINED PROCESSOR--

2. On page 29, lines 2-3 of the specification, please amend the title of the application as follows:

B2

-- METHOD AND APPARATUS FOR MULTI-MODE JUMP DELAY SLOT CONTROL IN A PIPELINED PROCESSOR--

3. On page 11, lines 25-27 of the specification, please amend the text as follows:

B3

--Table 3 illustrates a second embodiment of the jump delay slot modes of the invention utilizing [five] four jump delay slot modes ([four] plus [one] four reserved) based on three data bits within the IW:--

4. On page 13, lines 23-34 of the specification, please amend the text as follows:

B4

--It is also noted that the methods and apparatus of the present invention may be used in conjunction with ([either] alone or collectively) other methods of pipeline control and interlock including, inter alia, those disclosed in Applicant's co-pending U.S. Patent Application Serial No. 09/523,871 filed March 13, 2000 entitled "Method And Apparatus For Jump Control In A Pipelined Processor," as well as those disclosed in Applicant's co-pending U.S. Patent Application Serial No. 09/524,179 filed March 13, 2000 entitled "Method And Apparatus For Processor Pipeline Segmentation and Reassembly," both filed contemporaneously herewith, both being incorporated by reference herein in their entirety. Furthermore, various register encoding schemes, such as the "loose" register encoding described in Applicant's co-pending U.S. Patent Application Serial No. 09/524,178 filed March 13, 2000 entitled "Method and